# 12-Bit, 80Msps Wide Bandwidth ADC

## FEATURES

- **Sample Rate: 80Msps**
- **PGA Front End (2.25V$_{P-P}$ or 1.35V$_{P-P}$ Input Range)**
- **71.8dB SNR and 87dB SFDR (PGA = 0)**
- **70.2dB SNR and 87dB SFDR (PGA = 1)**
- **500MHz Full Power Bandwidth S/H**
- No Missing Codes
- Single 5V Supply
- Power Dissipation: 1.45W
- Two Pin Selectable Reference Values
- Data Ready Output Clock
- Pin Compatible 14-Bit 80Msps Device (LTC1750)
- 48-Pin TSSOP Package

## APPLICATIONS

- Direct IF Sampling
- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Communications Test Equipment
- Undersampling

## DESCRIPTION

The LTC®1749 is an 80Msps, 12-bit A/D converter designed for digitizing wide dynamic range signals up to frequencies of 500MHz. The input range of the ADC can be optimized with the on-chip PGA sample-and-hold circuit and flexible reference circuitry.

The LTC1749 has a highly linear sample-and-hold circuit with a bandwidth of 500MHz. The SFDR is 80dB with an input frequency of 250MHz. Ultralow jitter of 0.15ps$_{RMS}$ allows undersampling of IF frequencies with minimal degradation in SNR. DC specs include ±1LSB INL and no missing codes.

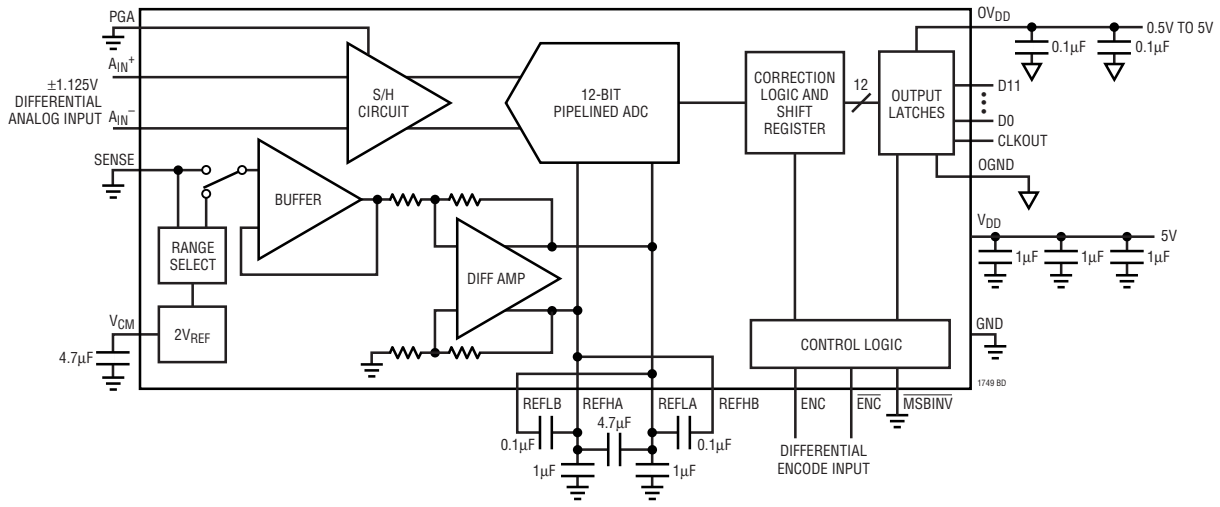
The digital interface is compatible with 5V, 3V, 2V and LVDS logic systems. The $\overline{ENC}$ and ENC inputs may be driven differentially from PECL, GTL and other low swing logic families or from single-ended TTL or CMOS. The low noise, high gain $\overline{ENC}$ and ENC inputs may also be driven by a sinusoidal signal without degrading performance. A separate output power supply can be operated from 0.5V to 5V, making it easy to connect directly to low voltage DSPs or FIFOs.

The 48-pin TSSOP package with a flow-through pinout simplifies the board layout.



## BLOCK DIAGRAM

**80Msps, 12-Bit ADC with a 2.25V Differential Input Range**

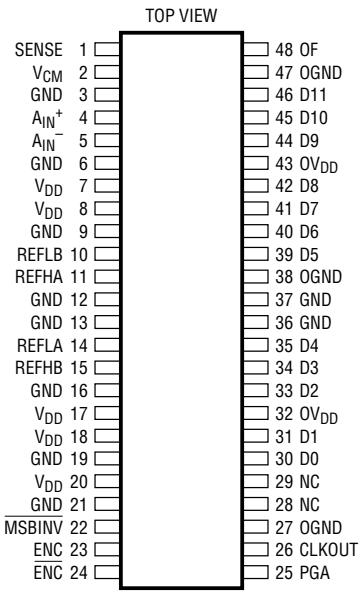


## ABSOLUTE MAXIMUM RATINGS

**$OV_{DD} = V_{DD}$ (Notes 1, 2)**

Supply Voltage ($V_{DD}$) ..... 5.5V
Analog Input Voltage (Note 3) .... –0.3V to ($V_{DD}$ + 0.3V)
Digital Input Voltage (Note 4) ..... –0.3V to ($V_{DD}$ + 0.3V)
Digital Output Voltage ..... –0.3V to ($V_{DD}$ + 0.3V)
OGND Voltage ..... –0.3V to 1V
Power Dissipation ..... 2000mW
Operating Temperature Range
LTC1749C ..... 0°C to 70°C
LTC1749I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




FW PACKAGE
48-LEAD PLASTIC TSSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 35°C/W

| ORDER PART NUMBER |
|---|
| LTC1749CFW |
| LTC1749IFW |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## CONVERTER CHARACTERISTICS

**The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution (No Missing Codes) | | ● | 12 | | | Bits |
| Integral Linearity Error | (Note 6) | <br>● | –1.0<br>–1.5 | ±0.4 | 1.0<br>1.5 | LSB<br>LSB |
| Differential Linearity Error | | ● | –0.8 | ±0.2 | 0.8 | LSB |
| Offset Error | (Note 7) External Reference ($V_{SENSE}$ = 1.125V, PGA = 0) | | –35 | ±8 | 35 | mV |
| Gain Error | External Reference ($V_{SENSE}$ = 1.125V, PGA = 0) | | –3.5 | ±1 | 3.5 | %FS |
| Full-Scale Tempco | Internal Reference<br>External Reference ($V_{SENSE}$ = 1.125V) | | | ±40<br>±20 | | ppm/°C<br>ppm/°C |
| Offset Tempco | | | | ±20 | | µV/°C |
| Input Referred Noise (Transition Noise) | $V_{SENSE}$ = 1.125V, PGA = 0 | | | 0.23 | | $LSB_{RMS}$ |

## ANALOG INPUT

**The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Analog Input Range (Note 8) | 4.75V ≤ $V_{DD}$ ≤ 5.25V | ● | | ±0.7 to ±1.125 | | V |
| $I_{IN}$ | Analog Input Leakage Current | 0 < $A_{IN}^+$, $A_{IN}^-$ < $V_{DD}$ | ● | –1 | | 1 | µA |
| $C_{IN}$ | Analog Input Capacitance | Sample Mode ENC < $\overline{ENC}$<br>Hold Mode ENC > $\overline{ENC}$ | | | 6.9<br>2.4 | | pF<br>pF |
| $t_{ACQ}$ | Sample-and-Hold Acquisition Time | | ● | | 5 | 6 | ns |
| $t_{AP}$ | Sample-and-Hold Acquisition Delay Time | | | | 0 | | ns |
| $t_{JITTER}$ | Sample-and-Hold Acquisition Delay Time Jitter | | | | 0.15 | | $ps_{RMS}$ |
| CMRR | Analog Input Common Mode Rejection Ratio | 1.5V < ($A_{IN}^-$ = $A_{IN}^+$) < 3V | | | 80 | | dB |

## DYNAMIC ACCURACY $T_A = 25°C$, $A_{IN} = -1dBFS$ (Note 5), $V_{SENSE} = V_{DD}$

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SNR | Signal-to-Noise Ratio | 5MHz Input Signal (PGA = 0)<br>5MHz Input Signal (PGA = 1) | | 71.8<br>70.2 | | dB<br>dB |
| | | 30MHz Input Signal (PGA = 0)<br>30MHz Input Signal (PGA = 1) | 70.5 | 71.7<br>70.2 | | dB<br>dB |
| | | 70MHz Input Signal (PGA = 0)<br>70MHz Input Signal (PGA = 1) | <br>68.8 | 71.4<br>70.1 | | dB<br>dB |
| | | 140MHz Input Signal (PGA = 1) | | 69.8 | | dB |
| | | 250MHz Input Signal (PGA = 1) | | 69.3 | | dB |
| | | 350MHz Input Signal (PGA = 1) | | 67.4 | | dB |
| SFDR | Spurious Free Dynamic Range | 5MHz Input Signal (PGA = 0) | | 87 | | dB |
| | | 5MHz Input Signal (PGA = 1) | | 87 | | dB |
| | | 30MHz Input Signal (PGA = 0) (HD2 and HD3) | 76 | 87 | | dB |
| | | 30MHz Input Signal (PGA = 0) (Other) | 83 | 90 | | dB |
| | | 70MHz Input Signal (PGA = 0) | | 85 | | dB |
| | | 70MHz Input Signal (PGA = 1) (HD2 and HD3) | 76 | 87 | | dB |
| | | 70MHz Input Signal (PGA = 1) (Other) | 83 | 90 | | dB |
| | | 140MHz Input Signal (PGA = 1) | | 84 | | dB |
| | | 250MHz Input Signal (PGA = 1) | | 80 | | dB |
| | | 350MHz Input Signal (PGA = 1) | | 74 | | dB |
| S/(N + D) | Signal-to-(Noise + Distortion) Ratio | 5MHz Input Signal (PGA = 0)<br>5MHz Input Signal (PGA = 1) | | 71.7<br>70.1 | | dB<br>dB |
| | | 30MHz Input Signal (PGA = 0)<br>30MHz Input Signal (PGA = 1) | | 71.6<br>70.0 | | dB<br>dB |
| | | 70MHz Input Signal (PGA = 0)<br>70MHz Input Signal (PGA = 1) | | 71.2<br>69.9 | | dB<br>dB |
| | | 250MHz Input Signal (PGA = 1) | | 68.6 | | dB |
| THD | Total Harmonic Distortion | 5MHz Input Signal, First 5 Harmonics (PGA = 0)<br>5MHz Input Signal, First 5 Harmonics (PGA = 1) | | –87<br>–87 | | dB<br>dB |
| | | 30MHz Input Signal, First 5 Harmonics (PGA = 0)<br>30MHz Input Signal, First 5 Harmonics (PGA = 1) | | –87<br>–87 | | dB<br>dB |
| | | 70MHz Input Signal, First 5 Harmonics (PGA = 0)<br>70MHz Input Signal, First 5 Harmonics (PGA = 1) | | –85<br>–87 | | dB<br>dB |
| | | 250MHz Input Signal (PGA = 1) | | 78 | | dB |
| IMD | Intermodulation Distortion | $f_{IN1}$ = 2.52MHz, $f_{IN2}$ = 5.2MHz (PGA = 0)<br>$f_{IN1}$ = 2.52MHz, $f_{IN2}$ = 5.2MHz (PGA = 1) | | –87<br>–87 | | dBc<br>dBc |
| | Sample-and-Hold Bandwidth | $R_{SOURCE}$ = 50Ω | | 500 | | MHz |

## INTERNAL REFERENCE CHARACTERISTICS (Note 5)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{CM}$ Output Voltage | $I_{OUT}$ = 0 | 1.95 | 2 | 2.05 | V |
| $V_{CM}$ Output Tempco | $I_{OUT}$ = 0 | | ±30 | | ppm/°C |
| $V_{CM}$ Line Regulation | 4.75V ≤ $V_{DD}$ ≤ 5.25V | | 3 | | mV/V |
| $V_{CM}$ Output Resistance | 1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA | | 4 | | Ω |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{DD}$ = 5.25V, $\overline{MSBINV}$ and PGA | | ● | 2.4 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD}$ = 4.75V, $\overline{MSBINV}$ and PGA | | ● | | | 0.8 | V |
| $I_{IN}$ | Digital Input Current | $V_{IN}$ = 0V to $V_{DD}$ | | ● | | | ±10 | µA |
| $C_{IN}$ | Digital Input Capacitance | $\overline{MSBINV}$ and PGA Only | | | | 1.5 | | pF |
| $V_{OH}$ | High Level Output Voltage | $OV_{DD}$ = 4.75V | $I_O$ = –10µA | | | 4.74 | | V |
| | | | $I_O$ = –200µA | ● | 4 | 4.74 | | V |
| $V_{OL}$ | Low Level Output Voltage | $OV_{DD}$ = 4.75V | $I_O$ = 160µA | | | 0.05 | | V |
| | | | $I_O$ = 1.6mA | ● | | 0.1 | 0.4 | V |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | | –50 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = 5V | | | | 50 | | mA |

## POWER REQUIREMENTS

**The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | | 4.75 | | 5.25 | V |
| $I_{DD}$ | Positive Supply Current | | ● | | 290 | 338 | mA |
| $P_{DIS}$ | Power Dissipation | | ● | | 1.45 | 1.69 | W |
| $OV_{DD}$ | Digital Output Supply Voltage | | | 0.5 | | $V_{DD}$ | V |

## TIMING CHARACTERISTICS

**The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 5)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_0$ | ENC Period | (Note 9) | ● | 12.5 | | 2000 | ns |
| $t_1$ | ENC High | (Note 8) | ● | 6 | | 1000 | ns |
| $t_2$ | ENC Low | (Note 8) | ● | 6 | | 1000 | ns |
| $t_3$ | Aperture Delay | (Note 8) | | | 0 | | ns |
| $t_4$ | ENC to CLKOUT Falling | $C_L$ = 10pF (Note 8) | ● | 1 | 2.4 | 4 | ns |
| $t_5$ | ENC to CLKOUT Rising | $C_L$ = 10pF (Note 8) | | | $t_1 + t_4$ | | ns |
| | For 80Msps 50% Duty Cycle | $C_L$ = 10pF (Note 8) | ● | 7.25 | 8.65 | 10.25 | ns |
| $t_6$ | ENC to DATA Delay | $C_L$ = 10pF (Note 8) | ● | 2 | 4.9 | 7.2 | ns |
| $t_7$ | ENC to DATA Delay (Hold Time) | (Note 8) | ● | 1.4 | 3.4 | 4.7 | ns |
| $t_8$ | ENC to DATA Delay (Setup Time) | $C_L$ = 10pF (Note 8) | | | $t_0 – t_6$ | | ns |
| | For 80Msps 50% Duty Cycle | $C_L$ = 10pF (Note 8) | ● | 5.3 | 7.6 | 10.5 | ns |
| $t_9$ | CLKOUT to DATA Delay (Hold Time), 80Msps 50% Duty Cycle | (Note 8) | ● | 6 | | | ns |
| $t_{10}$ | CLKOUT to DATA Delay (Setup Time), 80Msps 50% Duty Cycle | $C_L$ = 10pF (Note 8) | ● | 2.1 | | | ns |
| | Data Latency | | | | 5 | | cycles |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to GND (unless otherwise noted).

**Note 3:** When these pin voltages are taken below GND or above $V_{DD}$, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above $V_{DD}$ without latchup.

**Note 4:** When these pin voltages are taken below GND, they will be clamped by internal diodes. This product can handle input currents of >100mA below GND without latchup. These pins are not clamped to $V_{DD}$.

**Note 5:** $V_{DD}$ = 5V, $f_{SAMPLE}$ = 80MHz, differential ENC/$\overline{ENC}$ = $2V_{P-P}$ 80MHz sine wave, input range = ±1.125V differential, unless otherwise specified.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

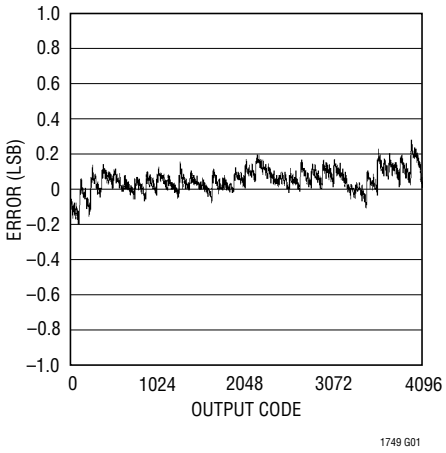
**Note 7:** Bipolar offset is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

**Note 8:** Guaranteed by design, not subject to test.

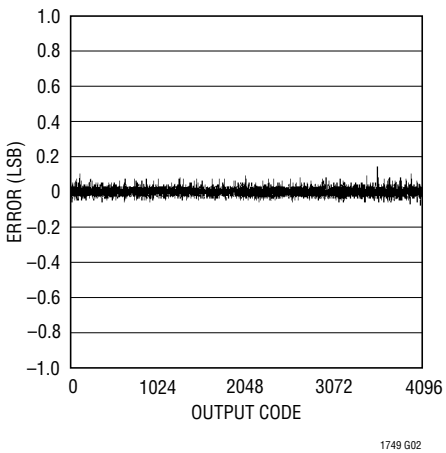
**Note 9:** Recommended operating conditions.

## TYPICAL PERFORMANCE CHARACTERISTICS

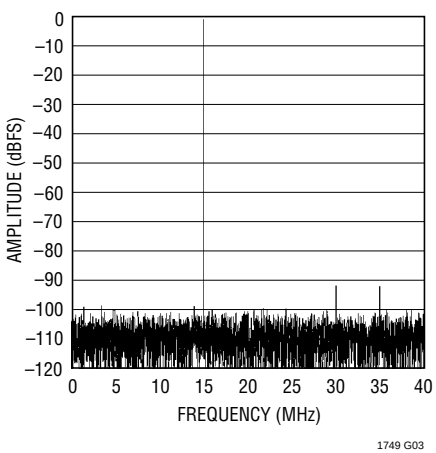
**INL**



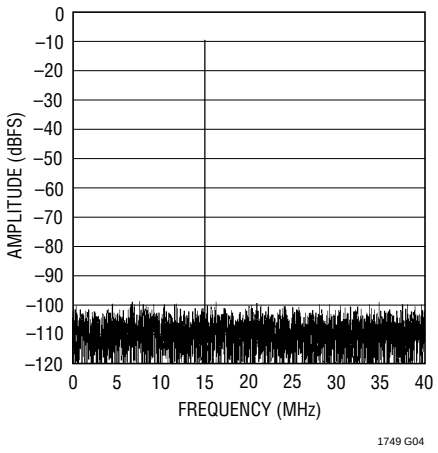

**DNL**



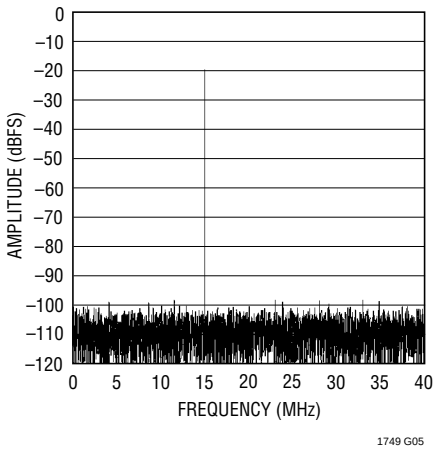

**8192 Point FFT, $f_{IN}$ = 15MHz, –1dB, PGA = 0**



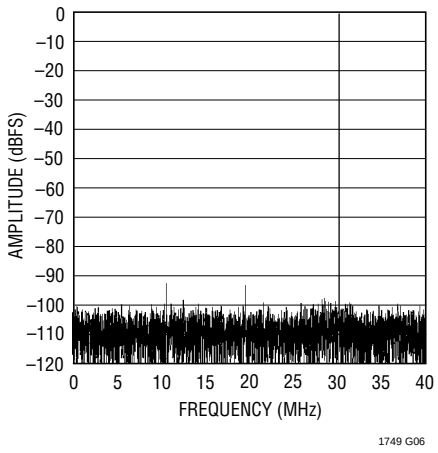

**8192 Point FFT, $f_{IN}$ = 15MHz, –10dB, PGA = 0**




**8192 Point FFT, $f_{IN}$ = 15MHz, –20dB, PGA = 0**

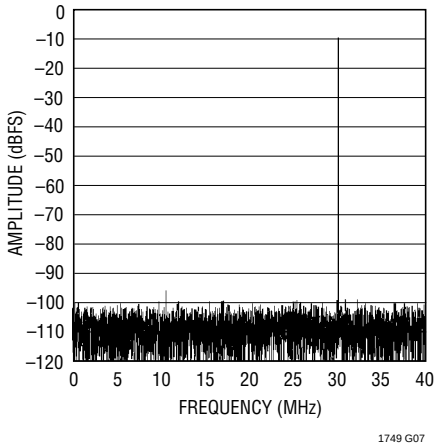



**8192 Point FFT, $f_{IN}$ = 30.2MHz, –1dB, PGA = 0**

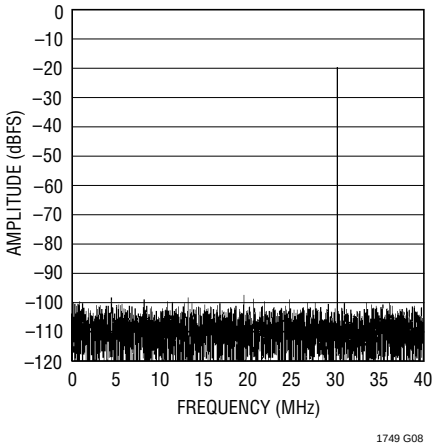


## TYPICAL PERFORMANCE CHARACTERISTICS

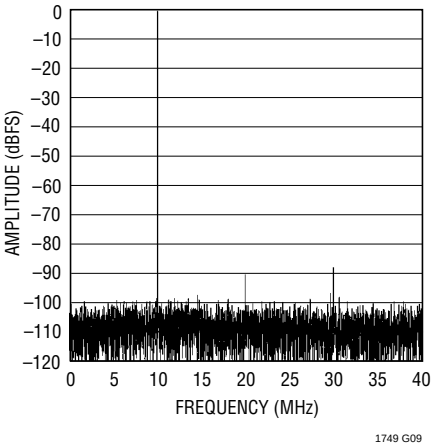
**8192 Point FFT, $f_{IN}$ = 30.2MHz, –10dB, PGA = 0**



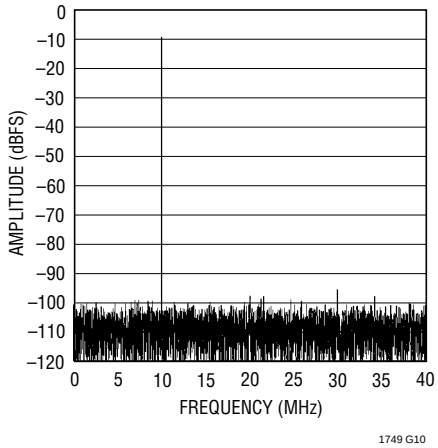

**8192 Point FFT, $f_{IN}$ = 30.2MHz, –20dB, PGA = 0**



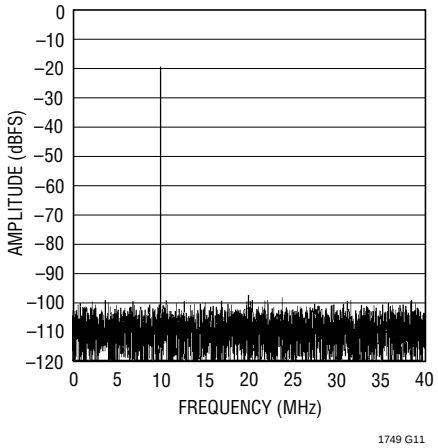

**8192 Point FFT, $f_{IN}$ = 70.03MHz, –1dB, PGA = 0**



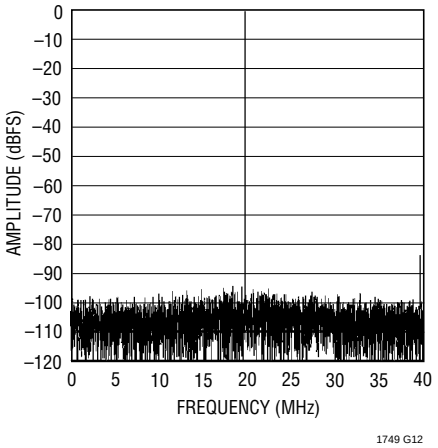

**8192 Point FFT, $f_{IN}$ = 70.03MHz, –10dB, PGA = 0**



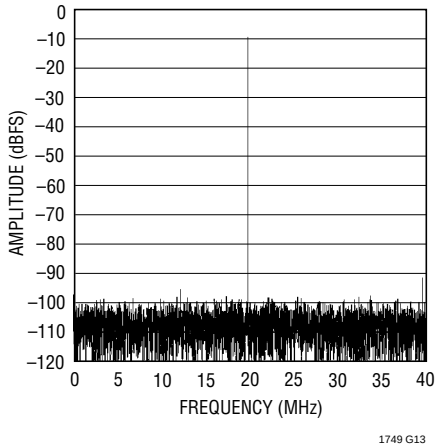

**8192 Point FFT, $f_{IN}$ = 70.03MHz, –20dB, PGA = 0**



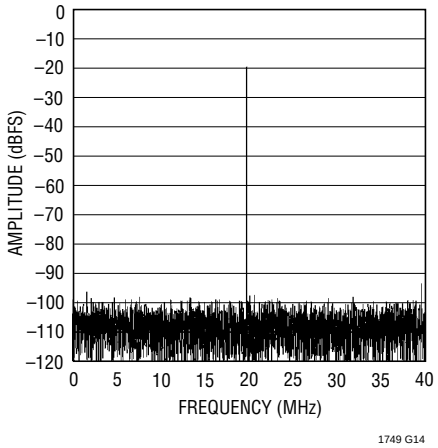

**8192 Point FFT, $f_{IN}$ = 140.2MHz, –1dB, PGA = 1**



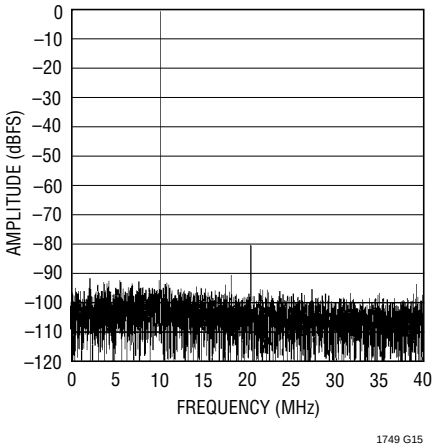

**8192 Point FFT, $f_{IN}$ = 140.2MHz, –10dB, PGA = 1**




**8192 Point FFT, $f_{IN}$ = 140.2MHz, –20dB, PGA = 1**

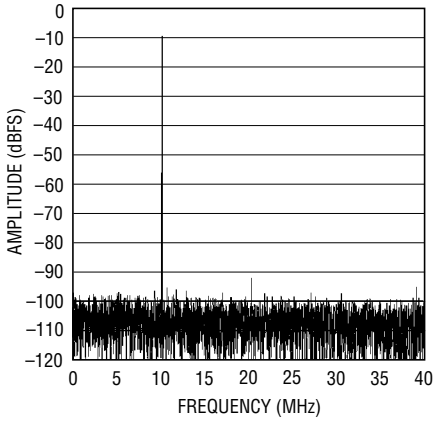



**8192 Point FFT, $f_{IN}$ = 250.2MHz, –1dB, PGA = 1**



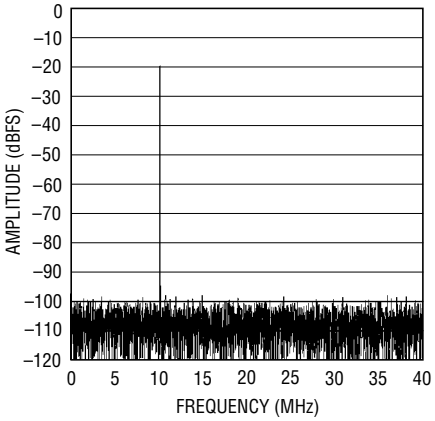
# TYPICAL PERFORMANCE CHARACTERISTICS

**8192 Point FFT, $f_{IN}$ = 250.2MHz, –10dB, PGA = 1**



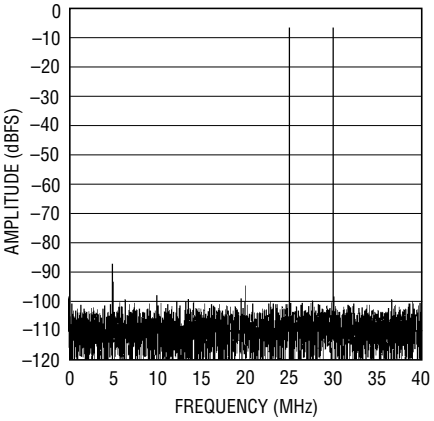

1749 G16

**8192 Point FFT, $f_{IN}$ = 250.2MHz, –20dB, PGA = 1**



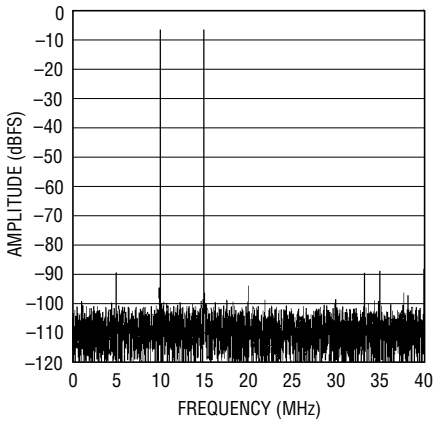

1749 G17

**8192 Point 2-Tone FFT, 25.01MHz and 30.1MHz, –7dB, PGA = 0**



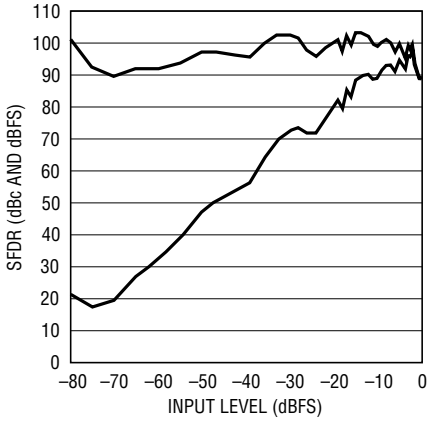

1749 G18

**8192 Point 2-Tone FFT, 65.01MHz and 70.01MHz, –7dB, PGA = 0**



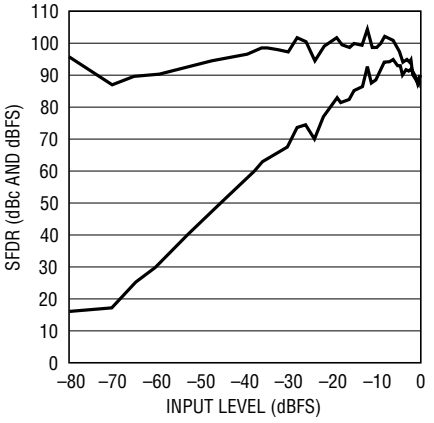

1749 G19

**SFDR vs 30.2MHz Input Level, PGA = 0**



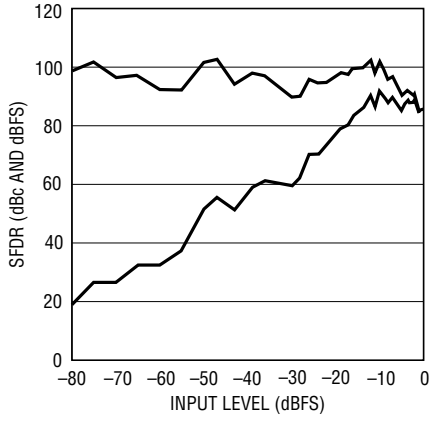

1749 G20

**SFDR vs 70.2MHz, Input Level, PGA = 0**



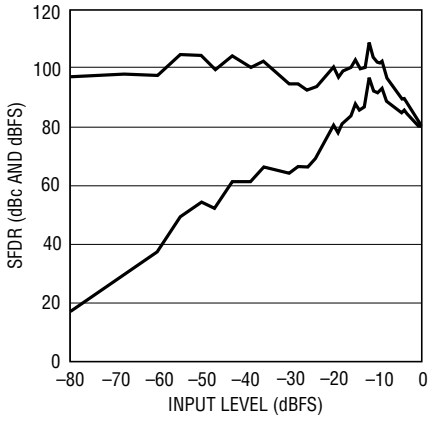

1749G21

**SFDR vs 140.2MHz, Input Level, PGA = 1**



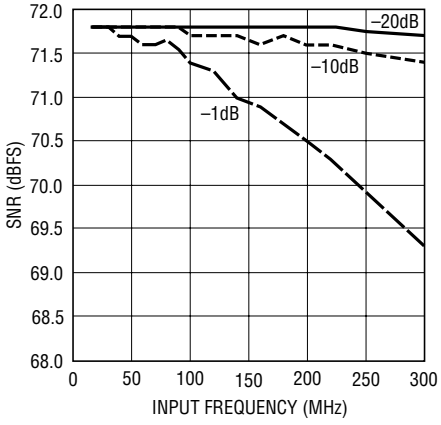

1749 G22

**SFDR vs 250.2MHz, Input Level**




1749 G23

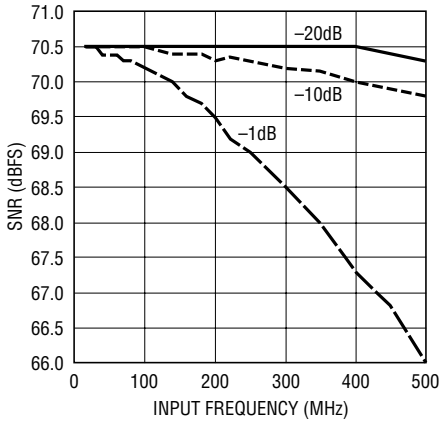
**SNR vs Input Frequency and Amplitude, PGA = 0**



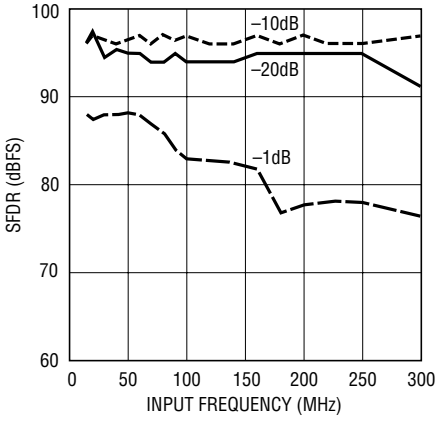

1749 G24

## TYPICAL PERFORMANCE CHARACTERISTICS

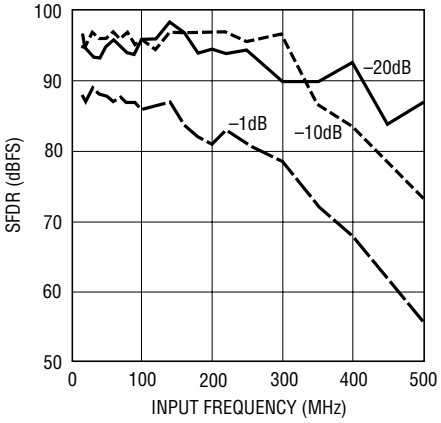
**SNR vs Input Frequency and Amplitude, PGA = 1**



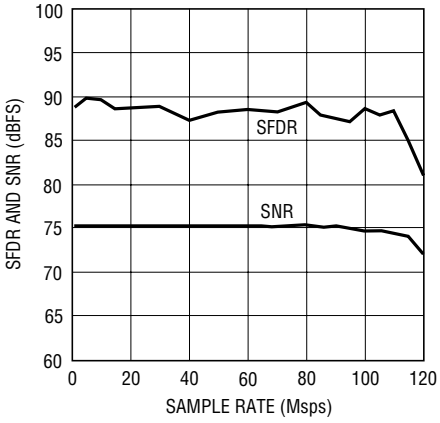

**SFDR (HD2 and HD3) vs Input Frequency and Amplitude, PGA = 0**



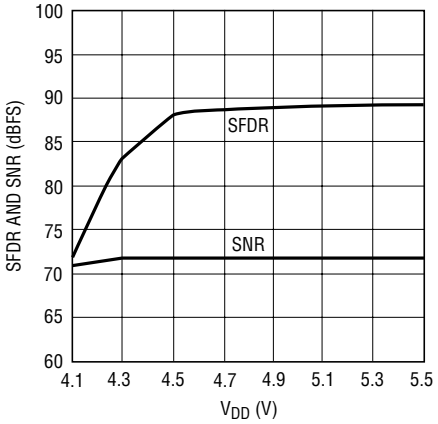

**SFDR (HD2 and HD3) vs Input Frequency and Amplitude, PGA = 1**



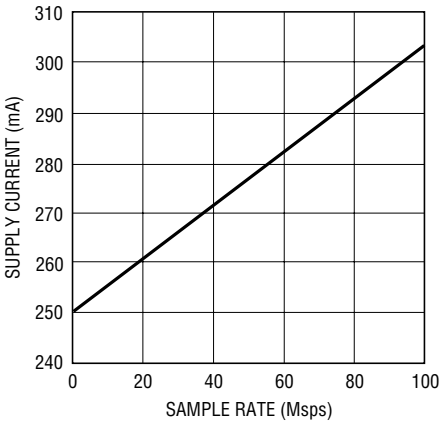

**SFDR and SNR vs Sample Rate, 15.2MHz, –1dB Input**




**SFDR and SNR vs $V_{DD}$, 15.2MHz, –1dB Input**




**Supply Current vs Sample Rate**



## PIN FUNCTIONS

**SENSE (Pin 1):** Reference Sense Pin. GND selects a $V_{REF}$ of 0.7V. $V_{DD}$ selects 1.125V. When $V_{SENSE}$ is between 0.7V and 1.125V, $V_{SENSE}$ is used as $V_{REF}$. The ADC input range is $\pm V_{REF}$/PGA gain.

**$V_{CM}$ (Pin 2):** 2.0V Output and Input Common Mode Bias. Bypass to ground with 4.7µF ceramic chip capacitor.

**GND (Pins 3, 6, 9, 12, 13, 16, 19, 21, 36, 37):** ADC Power Ground.

**$A_{IN}^+$ (Pin 4):** Positive Differential Analog Input.

**$A_{IN}^-$ (Pin 5):** Negative Differential Analog Input.

**$V_{DD}$ (Pins 7, 8, 17, 18, 20):** 5V Supply. Bypass to AGND with 1µF ceramic chip capacitors at Pin 8 and Pin 18.

**REFLB (Pin 10):** ADC Low Reference. Bypass to Pin 11 with 0.1µF ceramic chip capacitor. Do not connect to Pin 14.

**REFHA (Pin 11):** ADC High Reference. Bypass to Pin 10 with 0.1µF ceramic chip capacitor, to Pin 14 with a 4.7µF ceramic capacitor and to ground with 1µF ceramic capacitor.

**REFLA (Pin 14):** ADC Low Reference. Bypass to Pin 15 with 0.1µF ceramic chip capacitor, to Pin 11 with a 4.7µF ceramic capacitor and to ground with 1µF ceramic capacitor.

**REFHB (Pin 15):** ADC High Reference. Bypass to Pin 14 with 0.1µF ceramic chip capacitor. Do not connect to Pin 11.

**$\overline{\text{MSBINV}}$ (Pin 22):** MSB Inversion Control. Low inverts the MSB, 2's complement output format. High does not invert the MSB, offset binary output format.

**ENC (Pin 23):** Encode Input. The input sample starts on the positive edge.

**$\overline{\text{ENC}}$ (Pin 24):** Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1µF ceramic for single-ended ENCODE signal.

**PGA (Pin 25):** Programmable Gain Amplifier Control. Low selects an effective front-end gain of 1. High selects an effective gain of 1 2/3. The ADC input range is $\pm V_{REF}$/PGA gain.

**CLKOUT (Pin 26):** Data Valid Output. Latch data on the rising edge of CLKOUT.

**OGND (Pins 27, 38, 47):** Output Driver Ground.

**NC (Pins 28, 29):** No Internal Connection.

**D0, D1 (Pins 30, 31):** Digital Outputs.

**$OV_{DD}$ (Pins 32, 43):** Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

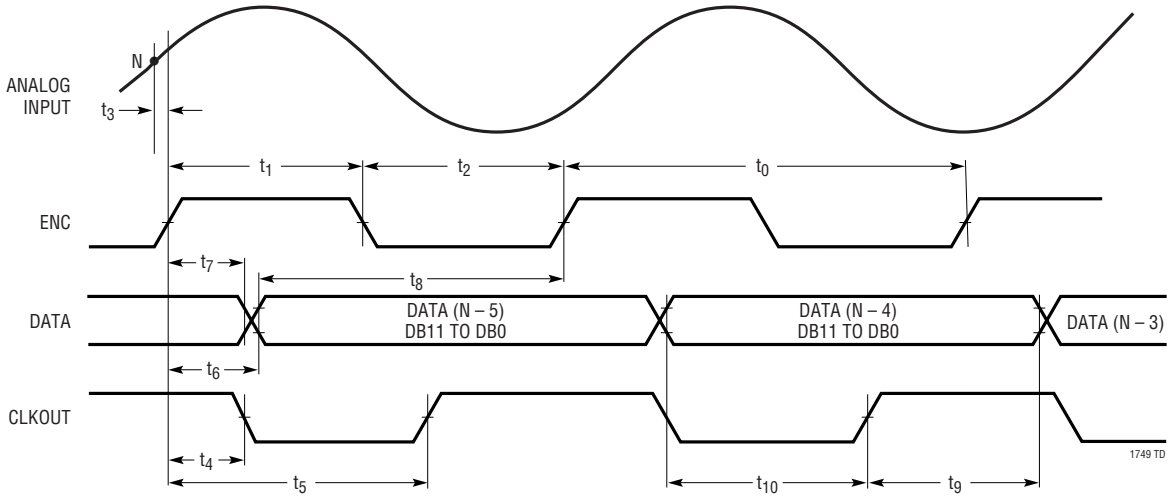
**D2-D4 (Pins 33 to 35):** Digital Outputs.

**D5-D8 (Pins 39 to 42):** Digital Outputs.

**D9-D11 (Pins 44 to 46):** Digital Outputs.

**OF (Pin 48):** Over/Under Flow Output. High when an over or under flow has occurred.

## TIMING DIAGRAM




## APPLICATIONS INFORMATION

### DYNAMIC PERFORMANCE

#### Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

#### Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

#### Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + ...Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

#### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

# APPLICATIONS INFORMATION

### Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

### Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

### Aperture Delay Time

The time from when a rising ENC equals the $\overline{ENC}$ voltage to the instant that the input signal is held by the sample and hold circuit.

### Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log(2\pi) \bullet F_{IN} \bullet T_{JITTER}$$

## CONVERTER OPERATION

The LTC1749 is a CMOS pipelined multistep converter with a front-end PGA. The converter has four pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later, see the Timing Diagram section. The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample-and-hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC1749 has two phases of operation, determined by the state of the differential ENC/$\overline{ENC}$ input pins. For brevity, the text will refer to ENC greater than $\overline{ENC}$ as ENC high and ENC less than $\overline{ENC}$ as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier.

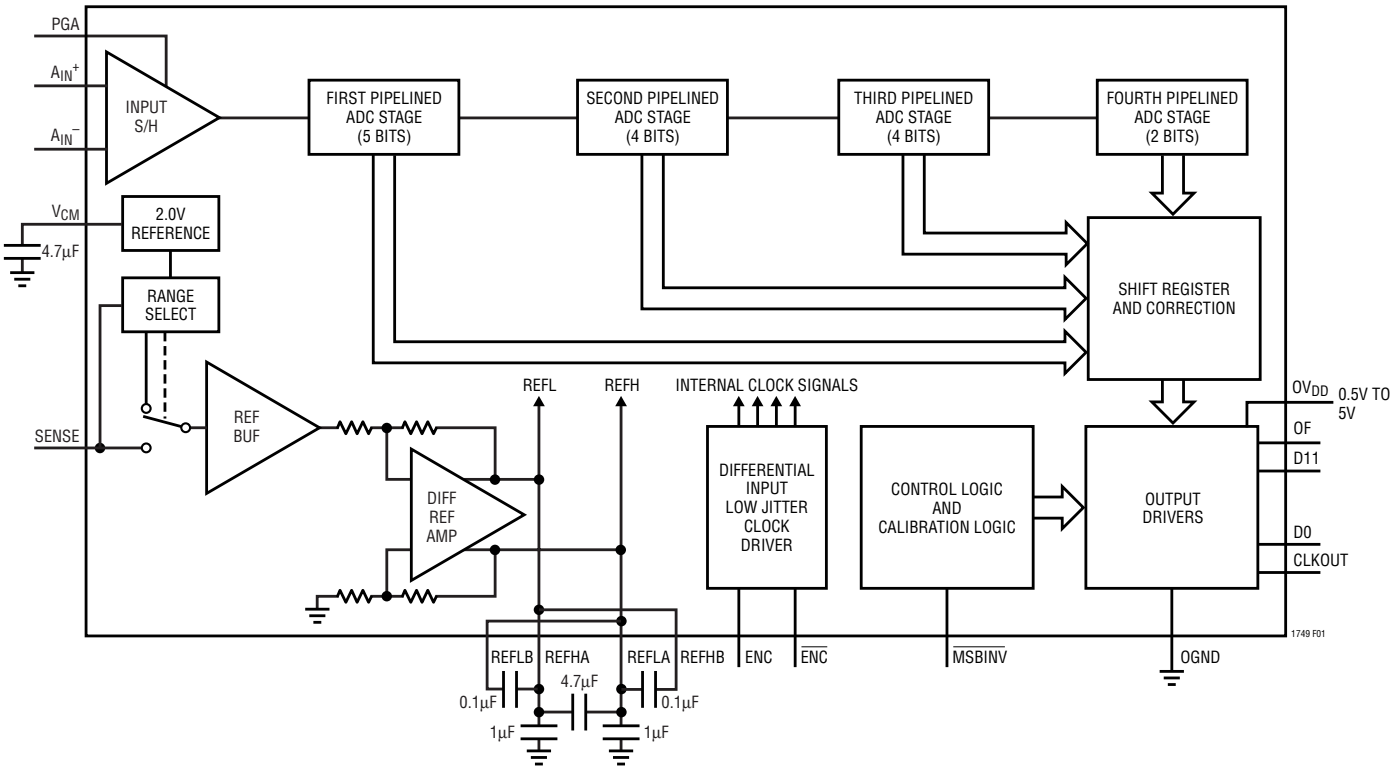



**Figure 1. Functional Block Diagram**

## APPLICATIONS INFORMATION

In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third stage, resulting in a third stage residue that is sent to the fourth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

### SAMPLE/HOLD OPERATION AND INPUT DRIVE

#### Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC1749 CMOS differential sample-and-hold. The differential analog inputs are sampled directly onto sampling capacitors ($C_{SAMPLE}$) through NMOS switches. This direct capacitor sampling results in lowest possible noise for a given sampling capacitor size. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC/$\overline{ENC}$ is low, the NMOS switch connects the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC/$\overline{ENC}$ transitions from low to high the

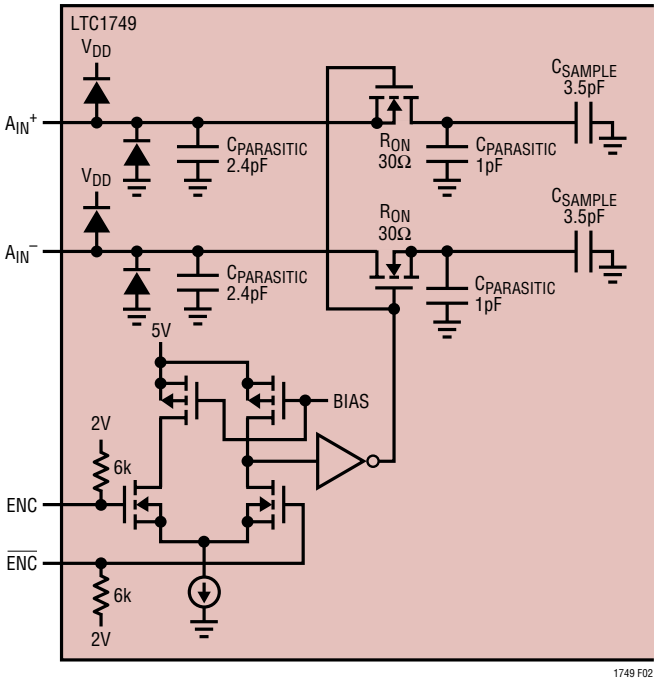



**Figure 2. Equivalent Input Circuit**

sampled input voltage is held on the sampling capacitors. During the hold phase when ENC/$\overline{ENC}$ is high the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC/$\overline{ENC}$ transitions from high to low the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

#### Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing within the valid input range, around a common mode voltage of 2.0V. The $V_{CM}$ output pin (Pin 2) may be used to provide the common mode bias level. $V_{CM}$ can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The $V_{CM}$ pin must be bypassed to ground close to the ADC with a 4.7µF or greater capacitor.

## APPLICATIONS INFORMATION

### Input Drive Circuits

The LTC1749 requires differential drive for the analog inputs. A balanced input drive will minimize even order harmonics that are due to nonlinear behavior of the input drive circuits and the S/H circuit.

The S/H circuit of the LTC1749 is a switched capacitor circuit (Figure 2). The input drive circuitry will see a sampling glitch at the start of the sampling period, when ENC/$\overline{\text{ENC}}$ falls. Although designed to be linear as possible, a small fraction of this glitch is nonlinear and can result in additional observed distortion if the input drive circuitry is too slow. For most practical circuits the glitch nonlinearity is more than 100dB below the fundamental. The glitch will decay during the sampling period with a time constant determined by the input drive and S/H circuitry.

For fast settling and wide bandwidth, a low drive impedance is required. The S/H bandwidth is partially determined by the source impedance. The full 500MHz bandwidth is valid for source impedance (each input) less than 30Ω. Higher source impedance can be used but full amplitude distortion will be better with a source impedance less than 100Ω.

### Transformers

Transformers provide a simple method for converting a single-ended signal to a differential signal; however, they have poor performance characteristics at low and high input frequencies. The lower –3dB corner of RF transformers can range from tens of kHz to tens of MHz. Operation near this corner results in poor 2nd order harmonic performance due to nonlinear transformer core behavior. The upper –3dB corner can vary from tens of MHz to several GHz. Operation near the upper corner can result in poor 2nd order performance due to poor balance on the secondary.

Transformers should be selected to have –3dB corners at least one octave away from the desired operating frequency. Transformers with larger cores usually have better performance at lower frequency and perform better when driving heavy loads.

Figure 3a shows the LTC1749 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC-biased with $V_{CM}$, setting the ADC input signal at its optimum DC level of 2V. In this example a 1:1 transformer is used; however, other transformer impedance ratios may be substituted.

Figure 3b shows the use of a transformer without a center tapped secondary. In this example the secondary is biased with the addition of two resistors placed in series across the secondary winding. The center tap of the secondary resistors is connected to the ADC $V_{CM}$ output to set the DC bias. This circuit is better suited for high input frequency applications since center tapped transformers generally have less bandwidth and poor balance at high frequencies than noncenter tapped transformers.

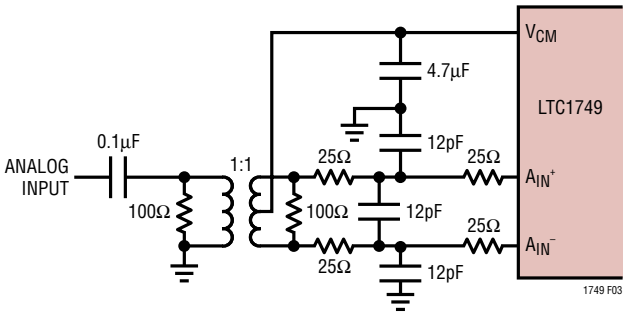



**Figure 3a. Single-Ended to Differential Conversion Using a Transformer**

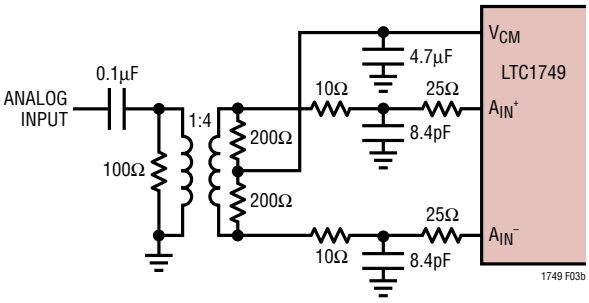



**Figure 3b. Using a Transformer Without a Center Tapped Secondary**

### Active Drive Circuits

Active circuits, open loop or closed loop, can be used to drive the ADC inputs. Closed-loop circuits such as op amps have excellent DC and low frequency accuracy but have poor high frequency performance. Figure 4 shows the dual LT®1818 op amp used for single-ended to differential signal conversion. Note that the two op amps do not have the same noise gain, which can result in poor balance at higher frequencies. The op amp configured in a gain of +1

## APPLICATIONS INFORMATION

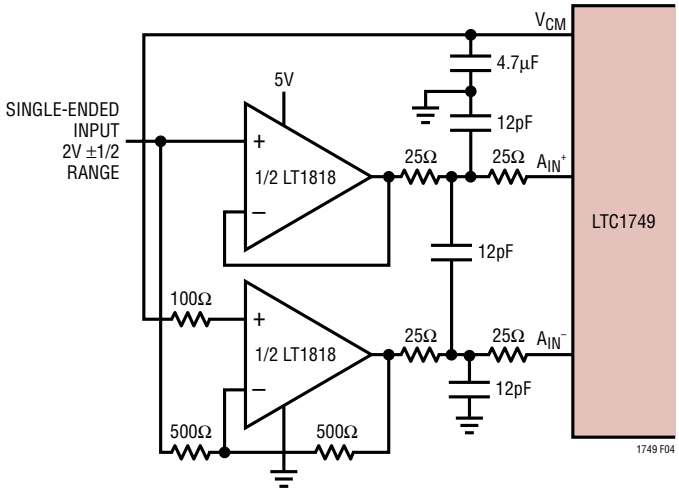



**Figure 4. Differential Drive with Op Amps**

can be configured in a noise gain of +2 with the addition of two equal valued resistors between the output and inverting input and between the two inputs. This however will raise the noise contributed by the op amps.

### Reference Operation

Figure 5 shows the LTC1749 equivalent reference circuitry consisting of a 2V bandgap reference, a 3-to-1 switch, a switch control circuit and a difference amplifier.

The 2V bandgap reference serves two functions. First, it is assessable at the $V_{CM}$ pin to provide a DC bias point for setting the common mode voltage of any external input circuitry. Second, it is used to derive internal reference levels that may be used to set the input range of the ADC. An external bypass capacitor is required for the 2V reference output at the $V_{CM}$ pin. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference, which will not be stable without this capacitor.

To achieve the optimal input range for an application, the internal reference voltage ($V_{REF}$) is flexible. The reference switch shown in Figure 5 connects $V_{REF}$ to one of two internally derived reference voltages, or to an externally derived reference voltage. The internally derived references are selected by strapping the SENSE pin to GND for 0.7V, or to $V_{DD}$ for 1.125V. When $0.7V > V_{SENSE} > 1.125V$,

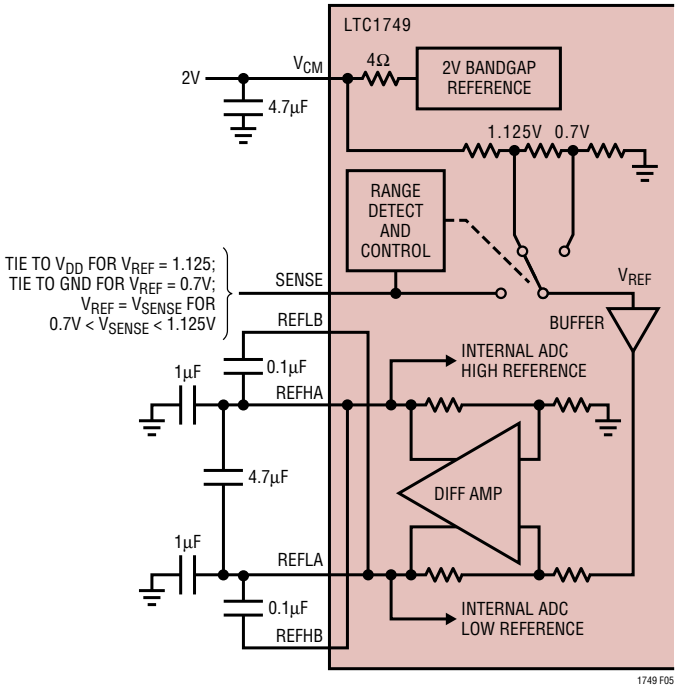



**Figure 5. Equivalent Reference Circuit**

$V_{SENSE}$ is directly connected to $V_{REF}$. Because of the dual nature of the SENSE pin, driving it with a logic device is not recommended.

Reference voltages between 0.7V and 1.125V may be programmed with two external resistors as shown in Figure 6a. An external reference may be used by applying its output directly or through a resistor divider to the SENSE pin (Figure 6b). When the SENSE pin is driven with an externally derived reference voltage, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor.

A difference amplifier generates the high and low references for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed. Each output has two pins: REFHA and REFHB for the high reference and REFLA and REFLB for the low reference. The doubled output pins are needed to reduce package inductance. Bypass capacitors must be connected as shown in Figure 5.

## APPLICATIONS INFORMATION

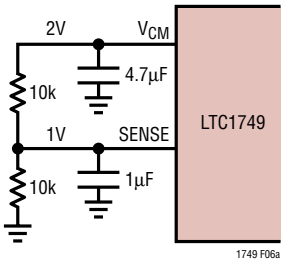



**Figure 6a. 2V Range ADC**

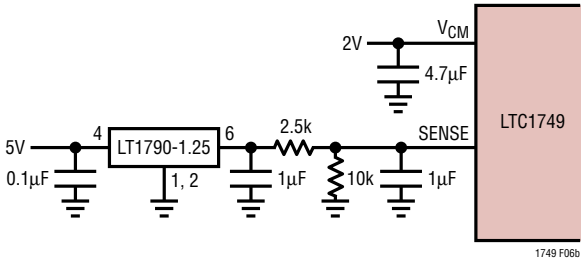



**Figure 6b. 2V Range ADC with External Reference**

### Input Range

The LTC1749 performance may be optimized by adjusting the ADC's input range to meet the requirements of the application. For lower input frequency applications (<40MHz), the highest input range of ±1.125V (2.25V) will provide the best SNR while maintaining excellent SFDR. For higher input frequencies (>80MHz), a lower input range will provide better SFDR performance with a reduction in SNR.

The input range of the ADC is determined as $\pm V_{REF}/A_{PGA}$, where $V_{REF}$ is the reference voltage (described in the Reference Operation section) and $A_{PGA}$ is the effective PGA gain. Table 1 shows the input range of the ADC versus the state of the two pins, PGA and SENSE.

### Driving the Encode Inputs

The noise performance of the LTC1749 can depend on the encode signal quality as much as on the analog input. The ENC/$\overline{\text{ENC}}$ inputs are intended to be driven differentially, primarily for immunity from common mode noise sources. Each input is biased through a 6k resistor to a 2V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.8V to $V_{DD}$. Each input may be driven from ground to $V_{DD}$ for single-ended drive.

**Table 1**

| PGA | $V_{SENSE}$ | INPUT RANGE | COMMENTS |
|---|---|---|---|
| 0 | = $V_{DD}$ | 2.25$V_{P-P}$ Differential | Best Noise, SNR = 71.8dB. Good SFDR, >80dB Up to 100MHz |
| 1 | = $V_{DD}$ | 1.35$V_{P-P}$ Differential | Improved High Frequency Distortion. SNR = 70.5dB. SFDR > 80dB Up to 250MHz |
| 0 | = GND | 1.4$V_{P-P}$ Differential | Reduced Internal Reference Mode with PGA = 0. Provides Similar Input Range as $V_{SENSE}$ = $V_{DD}$ and PGA = 0 But with Worse Noise. SNR = 70.3dB |
| 1 | = GND | 0.84$V_{P-P}$ Differential | Smallest Possible Input Span. Useful for Improved Distortion at Very High Frequencies, But with Reduced Noise Performance. SNR = 69dB |
| 0 | 0.7V < $V_{SENSE}$ < 1.125V | 2 × $V_{SENSE}$ Differential | Adjustable Input Range with Better Noise Performance. SNR = 71.8dB with $V_{SENSE}$ = 1.125V, SNR = 70.3dB with $V_{SENSE}$ = 0.7V |
| 1 | 0.7V < $V_{SENSE}$ < 1.125V | 1.2 × $V_{SENSE}$ Differential | Adjustable Input Range with Better High Frequency Distortion. SNR = 70.5dB with $V_{SENSE}$ = 1.125V, SNR = 69dB with $V_{SENSE}$ = 0.7V |

## APPLICATIONS INFORMATION

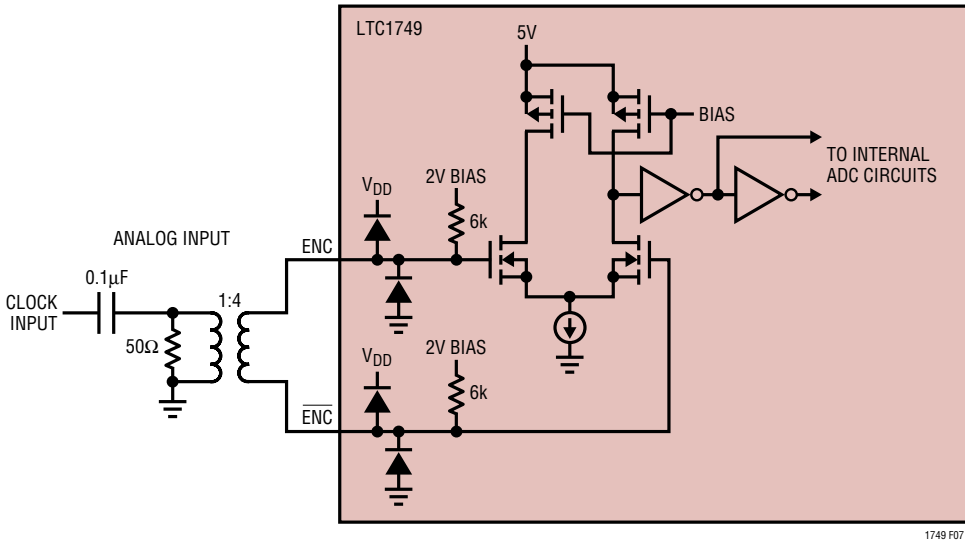



**Figure 7. Transformer Driven ENC/$\overline{ENC}$**

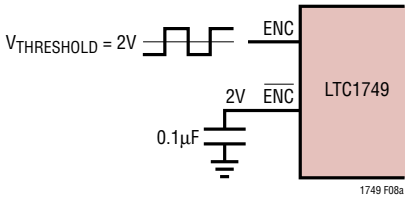



**Figure 8a. Single-Ended ENC Drive, Not Recommended for Low Jitter**

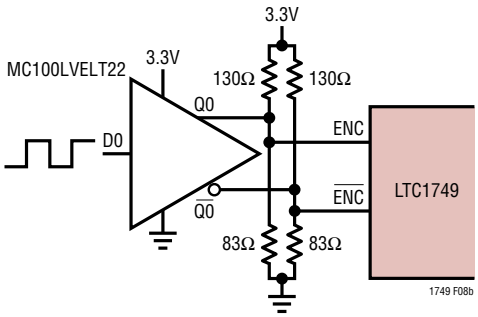



**Figure 8b. ENC Drive Using a CMOS-to-PECL Translator**

### Maximum and Minimum Encode Rates

The maximum encode rate for the LTC1749 is 80Msps. For the ADC to operate properly the encode signal should have a 50% (±4%) duty cycle. Each half cycle must have at least 6ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended encode signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

At sample rates slower than 80Msps the duty cycle can vary from 50% as long as each half cycle is at least 6ns.

The lower limit of the LTC1749 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC1749 is 1Msps.

### DIGITAL OUTPUTS

### Digital Output Buffers

Figure 9 shows an equivalent circuit for a single output buffer. Each buffer is powered by $OV_{DD}$ and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

## APPLICATIONS INFORMATION

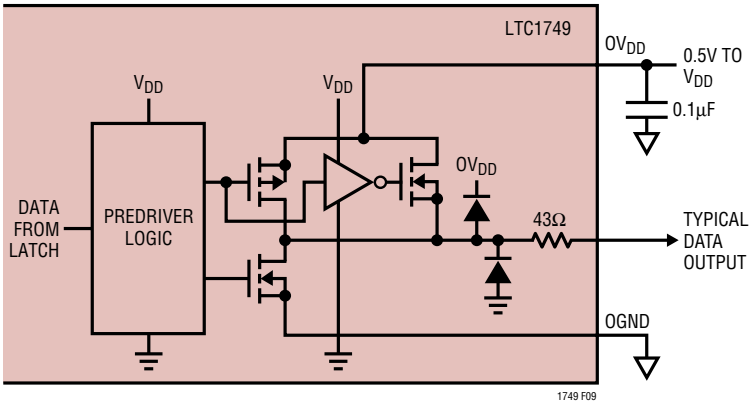



**Figure 9. Equivalent Circuit for a Digital Output Buffer**

### Output Loading

As with all high speed/high resolution converters the digital output loading can affect the performance. The digital outputs of the LTC1749 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

Lower $OV_{DD}$ voltages will also help reduce interference from the digital outputs.

### Format

The LTC1749 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the $\overline{MSBINV}$ pin; high selects offset binary.

### Overflow Bit

An overflow output bit indicates when the converter is overranged or underranged. When OF outputs a logic high the converter is either overranged or underranged.

### Output Clock

The ADC has a delayed version of the $\overline{ENC}$ input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data will be updated just after CLKOUT falls and can be latched on the rising edge of CLKOUT.

### Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, $OV_{DD}$, should be tied to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 3V supply then $OV_{DD}$ should be tied to that same 3V supply. $OV_{DD}$ can be powered with any voltage up to 5V. The logic outputs will swing between OGND and $OV_{DD}$.

## GROUNDING AND BYPASSING

The LTC1749 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. The pinout of the LTC1749 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the $V_{DD}$, $V_{CM}$, REFHA, REFHB, REFLA and REFLB pins as shown in the block diagram on the front page of this data

## APPLICATIONS INFORMATION

sheet. Bypass capacitors must be located as close to the pins as possible. Of particular importance are the capacitors between REFHA and REFLB and between REFHB and REFLA. These capacitors should be as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recomended. The large 4.7µF capacitor between REFHA and REFLA can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1749 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

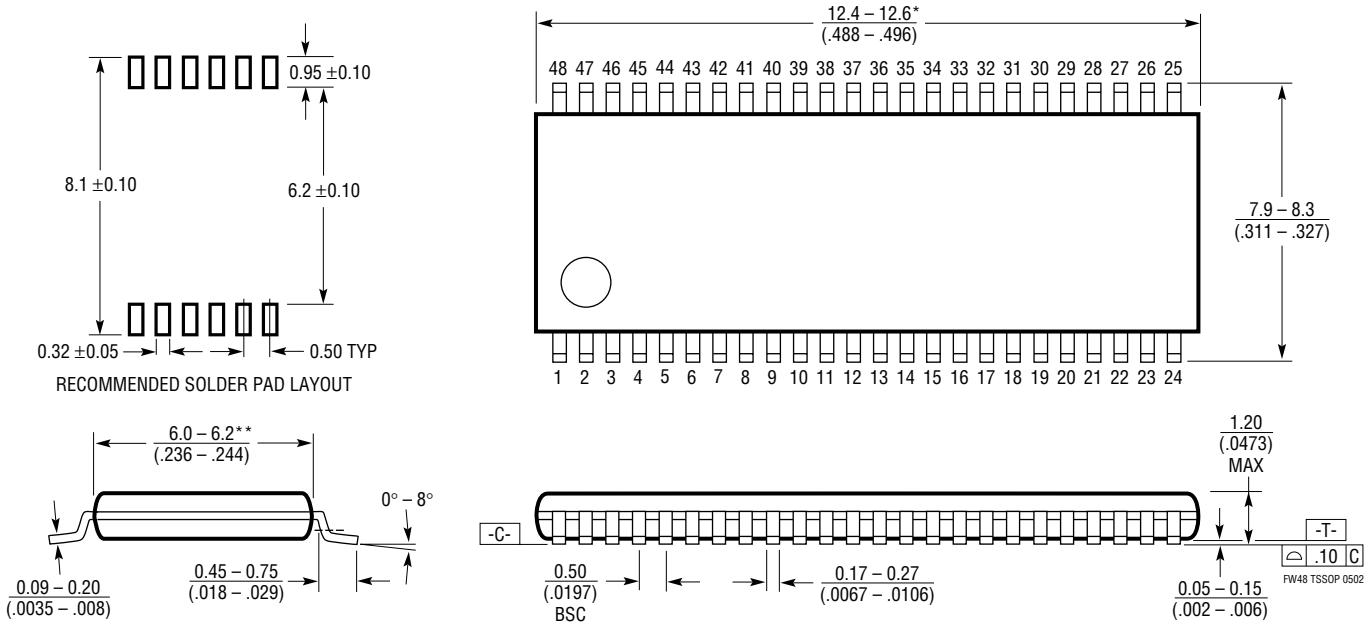
An analog ground plane separate from the digital processing system ground should be used. All ADC ground pins labeled GND should connect to this plane. All ADC $V_{DD}$ bypass capacitors, reference bypass capacitors and input filter capacitors should connect to this analog plane. The LTC1749 has three output driver ground pins, labeled OGND (Pins 27, 38 and 47). These grounds should connect to the digital processing system ground. The output driver supply, $OV_{DD}$ should be connected to the digital processing system supply. $OV_{DD}$ bypass capacitors should bypass to the digital system ground. The digital processing system ground should be connected to the analog plane at ADC OGND (Pin 38).

### HEAT TRANSFER

Most of the heat generated by the LTC1749 is transferred from the die through the package leads onto the printed circuit board. In particular, ground pins 12, 13, 36 and 37 are fused to the die attach pad. These pins have the lowest thermal resistance between the die and the outside environment. It is critical that all ground pins are connected to a ground plane of sufficient area. The layout of the evaluation circuit shown on the following pages has a low thermal resistance path to the internal ground plane by using multiple vias near the ground pins. A ground plane of this size results in a thermal resistance from the die to ambient of 35°C/W. Smaller area ground planes or poorly connected ground pins will result in higher thermal resistance.

# PACKAGE DESCRIPTION

**FW Package**
**48-Lead Plastic TSSOP (6.1mm)**
(Reference LTC DWG # 05-08-1651)




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1405 | 12-Bit, 5Msps Sampling ADC with Parallel Output | Pin Compatible with the LTC1420 |
| LTC1406 | 8-Bit, 20Msps ADC | Undersampling Capability up to 70MHz |
| LTC1411 | 14-Bit, 2.5Msps ADC | 5V, No Pipeline Delay, 80dB SINAD |
| LTC1412 | 12-Bit, 3Msps, Sampling ADC | ±5V, No Pipeline Delay, 72dB SINAD |
| LTC1414 | 14-Bit, 2.2Msps ADC | ±5V, 81dB SINAD and 95dB SFDR |
| LTC1420 | 12-Bit, 10Msps ADC | 71dB SINAD and 83dB SFDR at Nyquist |
| LT®1461 | Micropower Precision Series Reference | 0.04% Max Initial Accuracy, 3ppm/°C Drift |
| LTC1666 | 12-Bit, 50Msps DAC | Pin Compatible with the LTC1668, LTC1667 |
| LTC1667 | 14-Bit, 50Msps DAC | Pin Compatible with the LTC1668, LTC1666 |
| LTC1668 | 16-Bit, 50Msps DAC | 16-Bit Monotonic, 87dB SFDR, 5pV-s Glitch Impulse |
| LTC1741 | 12-Bit, 65Msps ADC | Pin Compatible with the LTC1743, LTC1745, LTC1747 |
| LTC1742 | 14-Bit, 65Msps ADC | Pin Compatible with the LTC1744, LTC1746, LTC1748 |
| LTC1743 | 12-Bit, 50Msps ADC | Pin Compatible with the LTC1741, LTC1745, LTC1747 |
| LTC1744 | 14-Bit, 50Msps ADC | Pin Compatible with the LTC1742, LTC1746, LTC1748 |
| LTC1745 | 12-Bit, 25Msps ADC | Pin Compatible with the LTC1741, LTC1743, LTC1747 |
| LTC1746 | 14-Bit, 25Msps ADC | Pin Compatible with the LTC1742, LTC1744, LTC1748 |
| LTC1747 | 12-Bit, 80Msps ADC | Pin Compatible with the LTC1741, LTC1743, LTC1745 |
| LTC1748 | 14-Bit, 80Msps ADC | Pin Compatible with the LTC1742, LTC1744, LTC1746 |
| LTC1750 | 14-Bit, 80Msps ADC with Wide Bandwidth | Pin Compatible with the LTC1749 |
| LT1807 | 325MHz, Low Distortion Dual Op Amp | Rail-to-Rail Input and Output |
| LT5512 | High Signal Level Down Converting Mixer | DC to 3GHz, 17dBm IIP3, Integrated LO Buffer |
| LT5515 | Direct Conversion Demodulator | 1.5GHz to 2.5GHz, 21.5dBm IIP3, Integrated LO Quadrature Generator |
| LT5516 | Direct Conversion Quadrature Demodulator | 800MHz to 3GHz, 17dBm IIP3, Integrated LO Buffer |
| LT5522 | High Signal Level Down Converting Mixer | 600MHz to 3GHz, 25dBm IIP3, Integrated LO Buffer |

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